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NOVEL 1-BIT FULL-ADDER CELL WITH ULTRA-LOW DELAY, PDP AND EDP

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ABSTRACT

The increasing demand for the high fidelity devices has laid emphasis on the development of high speed, low power and high performance systems. The 1-bit full-adder circuit is very important component in the design of application specific integrated circuits. This paper presents a novel ultra-low delay, PDP and EDP full-adder based on pass-transistor and TG techniques. The main advantage of this design is very low propagation delay, which leads to achieving lower PDP and EDP than 14T full adder. Intensive HSPICE simulation shows that the new full-adder consumes around 10.5% less power than 14T adder, moreover its propagation around delay 10% less than 14T full-adder. We have compared 14T full adder with proposed full-adder .Simulation has been carried out by HSPICE in 0.18µm technology at 1.8V supply voltage.

KEYWORDS: TG, Pass-Transistor, PDP, EDP

INTRODUCTION

With the explosive growth in laptops, portable personal communication systems, and the evolution of the shrinking technology, the research effort in low-power microelectronics has been intensified. Today, there are an increasing number of portable applications requiring small-area low-power high throughput. Therefore, circuits with low-power consumption become the major candidates for design of microprocessor and system-components [1-4]. Ever since its inception, the design of full-adders which forms the basic building blocks of all digital VLSI circuits has been undergoing a considerable improvement, being motivated by three basic design goals, viz. minimizing the transistor count, minimizing the power consumption and increasing the speed [9],[10]. In fact adder is the most frequently used unit in processors, for doing operations like add, subtract, multiply, and divide. One common technique for reducing power is power supply scaling. For CMOS circuits the cost of lower supply voltage is lower performance. Scaling the threshold voltage can limit this performance loss somewhat but results in increased leakage [5], [6]. Other techniques used in low power design include clock gating and dynamic voltage/frequency scaling [6-8]. Sub-threshold circuit design involves scaling the supply voltage below the threshold voltage, where load capacitances are charged/ discharged by sub-threshold leakage currents. Leakage currents are orders of magnitude lower than drain currents in the strong inversion regime, so there is a significant limit on the maximum performance of sub-threshold circuits. Therefore, traditionally, sub-threshold circuits have been used for applications which require ultra-low power dissipation, with low-to moderate circuit performance [6], [8]. The 1-bit full-adder design is one of the most critical components of a processor that determines its throughput, as it is used in ALU, the floating point unit, and address generation in case of cache or memory accesses[6],[8]. The total power dissipated in generic digital CMOS gate is calculated by Eq. (1), Eq. (2), Eq. (3), and Eq. (4).

$$P_{Total} = P_{Dynamic} + P_{Short\ Circuit} + P_{Static} \quad (1)$$

$$P_{Dynamic} = P.C_L.f.V_{DD}^2 \quad (2)$$

$$P_{Short\ Circuit} = I_{peak}.t_{SC}.V_{DD}.f \quad (3)$$

$$P_{Static} = I_{Static}.V_{DD} \quad (4)$$

The above equations P, f, C_L, V_{DD}, I_{peak}, t_{SC} and I_{Static} are respectively, change state probability of gate, simulation frequency, capacitor of gate, supply voltage, maximum current during changing the status of gate, short circuit time and static current. Static power is very important in low supply voltage.

Although lowering supply voltage and modifying the threshold voltage results in decreasing the power consumption, modifying V_{th} and reducing supply voltage have direct influence on latency of the circuit, and as shown in Eq. (5), and Eq. (6) any increase in V_{th} or decrease in supply voltage cause reduction in performance of the 2circuit [11], [12].

$$T_{Propagation}NMOS = T_{P_{H\to L}} \approx \frac{C_L.V_{DD}}{K_n(V_{DD} - V_{tn})^2} \quad (5)$$

$$T_{Propagation}PMOS = T_{P_{L\to H}} \approx \frac{C_L.V_{DD}}{K_p(V_{DD} - |V_{tp}|)^2} \quad (6)$$

The most important parameter for optimization of full-adder is energy delay product (EDP).

Many full-adders have been designed and published in literature. They are built upon different logic styles. Among these adders the circuits explained below will be used for comparison in this paper. Although all of them perform a similar function, but the method of producing the intermediate nodes and outputs, the loads on them and transistor count are varied. In all of these full-adders, it is tried to reduce power and delay factors and thus decrease power delay product(PDP) and energy delay product(EDP) in comparison to the each full-adder is presented. The remaining of the paper is organized as follows. Brief explain of 14T full-adder cell is in Section (II). Section (III) is present and describe of proposed full-adder (MGT adder). Section (IV) is present Simulation and Compare among MGT full-adder with 14T full-adder. Section (V) is present overall conclusions of this paper.

EXPLAIN ABOUT 14T FULL-ADDERS

14T full-adder is shown in Figure 1. It is incorporation of pass-transistor and TG techniques and it has 14 transistors in its structure. This full-adder has the least number of transistors among all full-adders in this paper moreover it has very low propagation delay, but its problem is high consumption power.

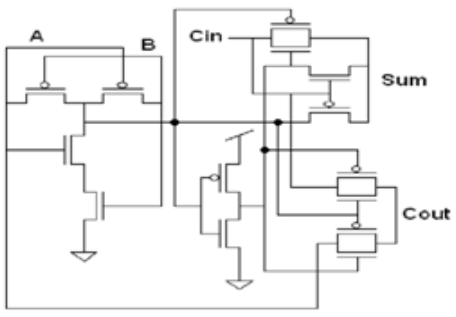

Figure 1: 114T Full-Adder

PROPOSED FULL-ADDER CELL (22T FULL-ADDER)

The proposed full-adder is utilized 22 transistors with minimum area. This adder is designed based two techniques pass-transistor and transmission gate. This full adder illustrate in Figure 2. In this design our effort was on reducing delay, PDP and EDP. In fact the most advantage of this adder is ultra-low propagation delay. This proposed adder has very low propagation delay and thus we intensive achieved the lowest power delay product (PDP) and energy delay product (EDP).

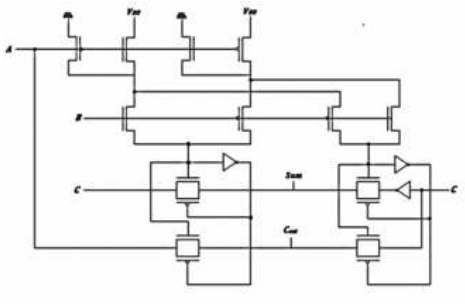

Figure 2: Proposed Full Adder Cell (22T Full-Adder)

SIMULATIONS AND RESULTS

In this section, the proposed circuit is evaluated and compared to the 14T full adder. The full-adder cells simulated using 0.18µm CMOS technology files with 100MHz and at 27^0C and the supply voltage is 1.8 V. Simulation result for full-adder in 0.18 µm technology with supply voltage and frequency 1.8V, 100MHz respectively.

Table 1

Design	Average Power (µw)	Delay (PS)	PDP (FJ)	EDP ($*10^{-27}$)	Tran. Count
14T	63.308	68	4.304944	292.736	14
Proposed Adder(22TAdder)	56.645	61.55	3.3633	207.017	22

So shown in Table 1 the 22T full-adder has the lower Delay, power consumption, power delay product (PDP) and energy delay product (EDP). In this design we could reduce area, Delay, PDP and EDP.

CONCLUSIONS

A novel ultra-low EDP and PDP 1-bit full-adder is proposed in this paper. This adder is based on TG and Pass-Transistor techniques. Ultra-low propagation delay, low power consumption, PDP and EDP are the four major features of the proposed adder cell (22T adder). As can be realized from the resulted information, 22T adder can improve power consumption, delay, PDP and EDP of full-adder. These results were obtained with simulation by HSPICE software at room temperature and supply voltage 1.8V.

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