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# NOVEL 1-BIT FULL-ADDER CELL WITH ULTRA-LOW DELAY, PDP AND EDP

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## ABSTRACT

The increasing demand for the high fidelity devices has laid emphasis on the development of high speed, low power and high performance systems. The 1-bit full-adder circuit is very important component in the design of application specific integrated circuits. This paper presents a novel ultra-low delay, PDP and EDP full-adder based on pass-transistor and TG techniques. The main advantage of this design is very low propagation delay, which leads to achieving lower PDP and EDP than 14T full adder. Intensive HSPICE simulation shows that the new full-adder consumes around 10.5% less power than 14T adder, moreover its propagation around delay 10% less than 14T full-adder. We have compared 14T full adder with proposed full-adder .Simulation has been carried out by HSPICE in 0.18µm technology at 1.8V supply voltage.

**KEYWORDS:** TG, Pass-Transistor, PDP, EDP