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ENHANCING ENERGY EFFICIENCY OF SRAM THROUGH OPTIMIZATION OF SRAM ARRAY STRUCTURES

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ABSTRACT

Reliability is a major concern in the microprocessor industry. SRAM plays a significant role in energy consumption due to increases in computing power. In order to get high efficiency in the SRAM, the array structure has to be modified. In traditional practices where SRAM array enclose more number of rows than columns. Previously proposed techniques improve the efficiency by 10% for 8kbit and 40% for 64kbit for same SRAM bit density and same supply voltage. The proposed techniques such as deep sub micron technology are implemented for getting better reliability. Many proposed design concern only on the low power dissipation but generally degrade response time. The power consumption of the system on chip devices having SRAMs increase largely with technology scaling because at low scale, Gate leakage current, sub threshold current, tunnelling plays a significant role in the SRAM operation. This work reveals that better SRAM energy efficiencies can be achieved with a wider SRAM array structure with fewer rows than columns particularly at low supply voltage. In this proposed 10T cell shows better performance with reduced power consumption and different Temperature as against conventional 8T SRAM.

KEYWORDS: Low Scale, Gate Leakage Current, Sub Threshold Current