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EMPLOYING POSITIVE FEEDBACK TECHNIQUE TO IMPROVE SIMULTANEOUSLY UGBW AND GAIN FOR OP-AMPS

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ABSTRACT

This paper presents a generally practical Positive Feedback Technique to increase simultaneously UGBW and dc gain of Op-Amps. Improvement on our first two-stage design, which has a UGBW of 281MHz and a 48dB gain, leads us to the proposed topology. Analysis proves that higher UGBW and dc gain seems sensible. Simulations verify the analysis and show an increased UGBW of 1GHz and dc gain of 65dB.

KEYWORDS: Op-Amp, Increase UGBW, Increase Gain, Positive Feedback

INTRODUCTION

Today, it is a worldwide electronics reality that Op-Amps with low power, high speed and high gain accompanied with unity gain bandwidth have turned to be an issue of expertise for designers.

Two stage Op-Amps in CMOS technology are more common, with the first stage being the differential input and the second one as class A or class AB inverting output [1]. One critical issue with regard to these Op-Amps can be poles and/or zeros in their transfer function, which degrade speed and other parameters like frequency performance. Consequently, two-stage op-amps require some form of compensation.

For compensation, we made use of Miller compensation method. In this technique a resistor is placed in series with a capacitor, and the pair connects the second stage to the first one. The resistor moves a right half-plane zero to the left half-plane. This offers the possibility of cancelling a pole by this zero choosing a proper amount for the resistance. By pole splitting, which is the main Miller's characteristic, Miller effect produces a dominant pole [2].

The struggle for increasing simultaneously unity gain bandwidth and gain seems to be continuous for long. In this paper we present one way of achieving this goal through Positive Feedback Technique, with no change in the size and values of the circuit elements. Then we can observe an increase in unity gain bandwidth and dc gain of the proposed design.

This paper includes the following sections: section II describes the proposed design and a concise analysis. Section III presents the simulation results. Finally, section IV concludes the paper.

PROPOSED OP-AMP

The proposed double ended Op-Amp is shown in Figure 2. As seen, it has two stages; the first stage is differential and the second one is in common source mode. The proposed design based on conventional Op-Amp is depicted in Figure 1, with the difference that two feedback paths have been added. One feedback is from Vout+ to the body of transistor M6, and another from Vout- to the body of transistor M5. Each of these paths gives the related body a higher DC voltage value than its corresponding source, leading to an increase in VBS. Such an increase results in reduction in the threshold voltage of M5 and M6 and increment in gm5 and gm6. It is obvious that any decrease in threshold voltage leads

to the enhancement of ID, and because the DC voltage value of nodes Vout- and Vout+ that bias the body of transistors M5 and M6, respectively, the threshold voltage of M5 and M6 decrease significantly proportional to when a feedback is not employed. With this condition we expect a significant increase in ID of transistors M5 and M6. On the other hand M5 and M6 are in series with M7 and M8, and this current flows from M7 and M8 too, but because M7 and M8 cannot provide this current, the performance of the circuit degrades

In order to eliminate this problem we connect gate to its own bulk in each of transistor M7 and M8. This results in body voltage M7 and M8 lower than VDD, leading to reduction in the threshold voltage of M7 and M8, hence ID of transistor M7 and M8 increases. As a result, an adequate amount of ID for transistors M5 and M6 is provided. Bipolar systems with PN open circuit connections

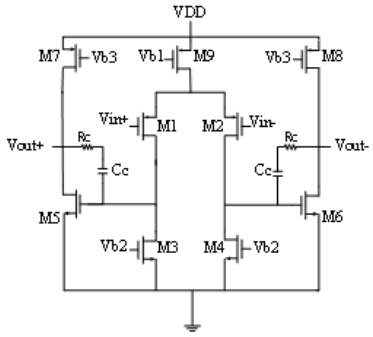

Figure 1: A Conventional Two-Stage Op-Amp

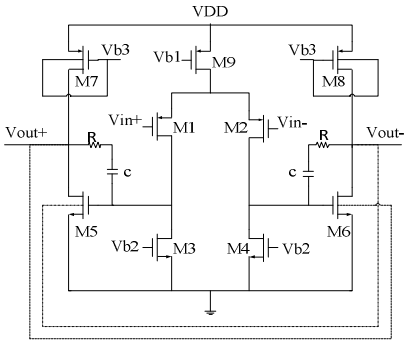

Figure 2: Proposed Op-Amp Structure

As seen in (1), and presented by[3], since gm5 and gm6 in the proposed Op-Amp increase proportional to the conventional Op-Amp in Figure 1, the second pole of the proposed Op-Amp move to a higher frequency. Thus the unity gain bandwidth of the proposed Op-Amp enhances.

$$P_2 \approx \frac{G_{m2}}{C_L} \tag{1}$$

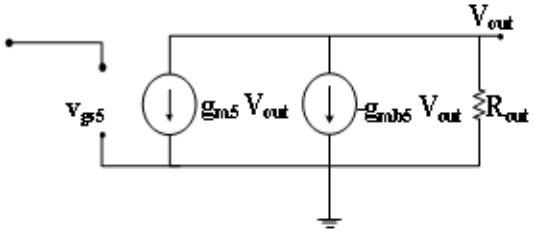

Figure 3: Small-Signal Equivalent Circuit of the Second Stage of the Proposed Op-Amp

In order to increase gain, one point is to be considered; that is the feedback paths must be established from the node to the bulk of M5/M6 so that this node and the source of M5/M6 become in phase. Consequently, to obtain a higher gain, the nodes Vout- and Vout+ are connected to the bulk of M5 and M6, respectively. Therefore, small-signal voltage vbs of M5 and M6 are equal to Vout- and Vout+, respectively. Figure 3 shows the small-signal equivalent circuit of the second stage of the proposed Op-Amp. The voltage gain of the second stage is presented in (2) and the total voltage gain, Rout1, and Rout2 of the proposed Op-Amp is treated in (3)-(5), respectively.

$$A_{v2} = \frac{g_{m5}R_{out2}}{1-g_{mb5}R_{out2}} \quad (2)$$

$$A_{VT} = g_{m1}R_{out1}\frac{g_{m5}R_{out2}}{1-g_{mb5}R_{out2}} \quad (3)$$

$$R_{out1} = r_{ds1} \| r_{ds3} \quad (4)$$

$$R_{out2} = r_{ds5} \| r_{ds7} \quad (5)$$

SIMULTION RESULTS

After completing the process of design for both the conventional and proposed Op-Amps, we employed Hspice in a 0.18µm CMOS technology for the simulation stage. The supply voltage of the Op-Amps is 1.8V. Aspect ratios of transistors and values of other circuit elements for both conventional and proposed designs are summarized in table 1. The frequency responses of both the conventional and proposed Op-Amps are depicted in Figures 3 and 4. As the simulation results show, the unity gain frequency has significantly increased from 281MHz in the conventional Op-Amp to 1GHz in the proposed Op-Amp, while the dc gain of the proposed Op-Amp has increased from 48dB in the conventional Op-Amp to 64dB in the proposed Op-Amp. The size of the transistors and other circuit elements are kept unchanged. Also the simulation results indicate a phase margin of 44 degrees for the conventional Op-Amp and 66 degrees for the proposed one.

Table 1: Aspect Ratios of Transistors and Values of Other Circuit Elements for Both Conventional and Proposed Designs

Parameter	Value
$(W/L)_{3,4}$	$4\times 60\ \mu m/0.18\ \mu m$
$(W/L)_{3,4}$	$3\times 60\ \mu m/0.18\ \mu m$
$(W/L)_{5,6}$	$2\times 75\ \mu m/0.18\ \mu m$
$(W/L)_{7,8}$	$2\times 10\ \mu m/0.18\ \mu m$
$(W/L)_{9}$	$2\times 90\ \mu m/0.18\ \mu m$
R_C	$350\ \Omega$
C_C	$4\ pF$
C_L	$2\ pF$

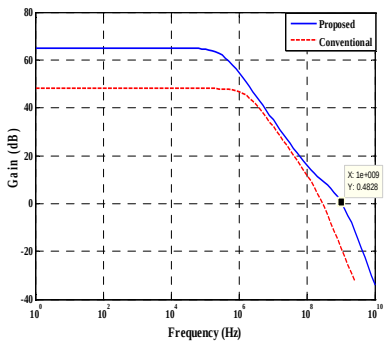

Figure 4: The Amplitude of the Voltage Gain for Both Conventional and Proposed Op-Amps

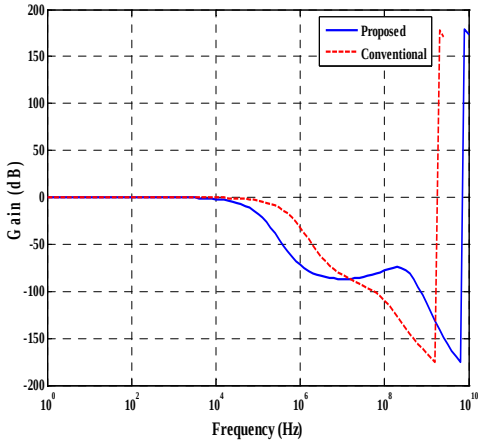

Figure 5: The Phase of the Voltage Gain for Both Conventional and Proposed Op-Amps

Table 2: Specifications of the Conventional and Proposed Op –Amps

Parameter	Conventional	Proposed
Supply voltage	1.8 V	1.8 V
Technology	0.18 μm	0.18 μm
Dc gain	48.12 dB	65 dB
UGBW	281 MHz	1 GHz
Phase margin	44°	66°

CONCLUSIONS

In this paper the design and simulation of two 1.8V Op-Amps in a 0.18μm CMOS technology was presented. Through analysis it was proved that increasing the UGBW and dc gain is feasible. Because the size of transistors in the proposed and the conventional designs are the same, the two circuits are readily comparable. The simulation results verify that the UGBW of the conventional Op-Amp has improved significantly from 281MHz to 1GHz, in the proposed Op-Amp, while the dc gain increase from 48dB to 65dB. Besides, the PM was improved from the primary value of 44° to 66°, almost with no difficulty.

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